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SELF-HEATING EFFECTS IN SILICON NANOSCALE MOSFET
(A MULTISCALE MODELING APPROACH)

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A b s t r a c t: In this work we present a novel multiscale simulation approach that combines circuit level with device level simulations together with experimental measurements to uncover the temperature of the hot-spot at nanoscale MOSFET devices. The circuit level simulation is performed with COMSOL simulation software. This allows one to perform electro-thermal modeling given the input Joule heating terms, the magnitude and the location of which is determined with more physically-based electro-thermal Monte Carlo device simulator. Simulation results obtained with this simulator are in agreement with experimental measurements from IMEC using specialized heater-sensor test structures in common-source and common-drain configurations.

Key words: electro-thermal modelling; self-heating effects; hot-spot temperature; nanoscale MOSFET devices; multiscale modeling

ЕФЕКТИ НА САМОЗАГРЕВАЊЕ КАЈ СИЛИЦИУМСКИ НАНОМЕТАРСКИ МОСФЕТ
(ПОВЕЌЕНИВОВСКО МОДЕЛИРАЊЕ)

А п с т р а к т: Во овој труд е презентиран нов пристап на т.н. симулација на повеќе нивоа со која се комбинираат симулацијата на ниво на електрично коло и симулацијата на ниво на електронски елемент со експериментални мерења, за да се определи температурата на жешката дамка кај нанометарските MOS-транзистори. Симулацијата на ниво на електрично коло се реализира со помош на комерцијалниот софтверски пакет COMSOL, кој овозможува да се направи електротермичка анализа ако се зададе како влезен параметар Џуловото загревање. Вредноста и локацијата на Џуловото загревање можат да се определат со изработениот електротермички Монте-Карло симулатор на електронски елементи. Резултатите од симулацијата добиени со овој симулатор се во согласност со експерименталните мерења на IMEC, користејќи структура составена од два *n*-канални мосфета во конфигурација на заеднички извор и во конфигурација на заеднички канал.

Клучни зборови: електротермичко моделирање; ефекти на самозагревање; температура на жешка дамка; нанометарски MOSFET; повеќенивовско моделирање

1. INTRODUCTION

For several decades, the ability of the semiconductor industry to follow Moore's law [1] has been the driving force of an incredible cycle: through transistor scaling one obtains a better performance-to-cost ratio for integrated circuits, which has resulted in an exponential growth of the semiconductor market. This, allows further investments in new technologies which enable further scaling. Scaling in turn, enables creation of more complex, faster, cheaper and low-power ICs. But, this essential engine that made the exponential growth possible is

now in considerable danger. Even with new approaches for the technology roadmap, known as 'more-than-Moore' scaling [2], which involves parallelism and improving efficiency at all technology levels – architecture, software and devices, thermal-power challenges and increasingly expensive energy demands still pose threats to the rate of increase in computer performance (Figure 1). Many of the transistors must be powered-down at any given time to meet the power budget. Also, even though scaling allows a decrease in the power per transistor, the number of transistors on a chip is increasing faster than the power requirements are falling [3].

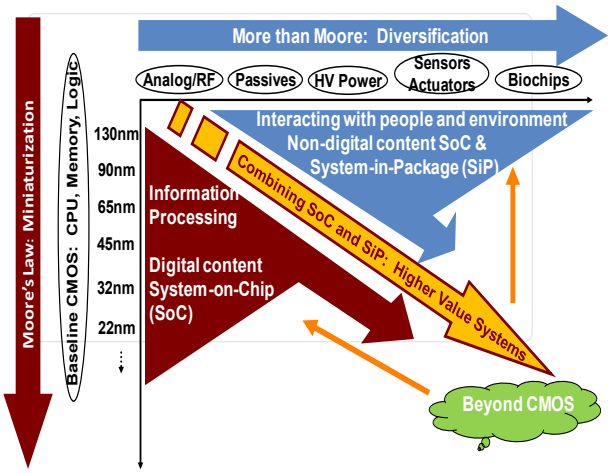

Fig. 1. More Moore and More-than-Moore scaling

The continuous miniaturization trend in microelectronic design has pushed the transistor gate length to a range of tens of nanometers. The downscaling of MOSFET devices is not without problems, however. It has necessitated the use of high-k dielectrics, strain and alternative device designs such as fully-depleted SOI devices, dual-gate structures, FinFETs, etc. Increasing power dissipation and decreasing device dimensions also exacerbates device self-heating effects, causing an overall degradation of the on-current due to the characteristic phonon hot-spot near the drain end of the device, which does not scale proportionally [4].

The study of heat transport and dissipation at the device level is becoming an essential part of the overall thermal design [5–7]. Due to the higher electric potential field and electron thermalization close to the drain, temperature non-uniformity peaks in the transistor drain region [8]. Drastic changes in both, electrical current flow and the thermal heat flow to the heat sink can be caused by this localized temperature non-uniformity. Ballistic transport that happens when gate length approaches the phonon mean free path changes the temperature distribution [9–10].

The need for the separate consideration of the optical phonon and the acoustic phonon bath comes from the very nature how the energy is transferred from the electron system to the lattice [11–12]. With the application of a drain bias, electrons gain energy from the lateral electric field and interact with both the optical phonon and the acoustic phonon bath (Figure 2). Since zone center optical phonons involved in the process have much larger energy than the acoustic phonons, most of the electron energy is stored as heat in the optical phonon bath. The zone center optical phonons have nearly zero group velocity, and the transfer of heat to acoustic phonons via anharmonic decay (three and four phonon processes) is relatively slow. Therefore, a hot-spot forms. The elevated temperature in the active region of the device leads to enhanced phonon scattering, and therefore, mobility and current reduction. This effect is called self-heating.

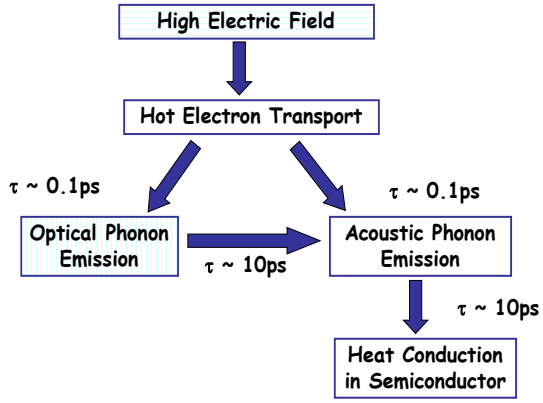

Fig. 2. The most likely path between energy carrying particles in a semiconductor device is shown together with the corresponding scattering time constants. About 80% of the heat is transferred to the lattice via the optical phonons and only 20% goes directly to the acoustic phonons

Understanding what is the value of the hot-spot temperature still remains an issue as direct measurements are not possible. Therefore, a combination of experiment with an accurate modeling technique is a must in order to determine the temperature of the hot-spot. In this work we present a novel multi-scale simulation approach that combines circuit level with device level simulations together with experimental measurements to uncover the temperature of the hot-spot in nanoscale MOSFET. The circuit level **simulation is performed** with COMSOL (or

Silvaco Giga 3D) simulation software. This allows one to perform electro-thermal modeling given the input Joule heating terms, the magnitude and the location of which is determined with more physically-based electro-thermal Monte Carlo device simulator (see Figure 3).

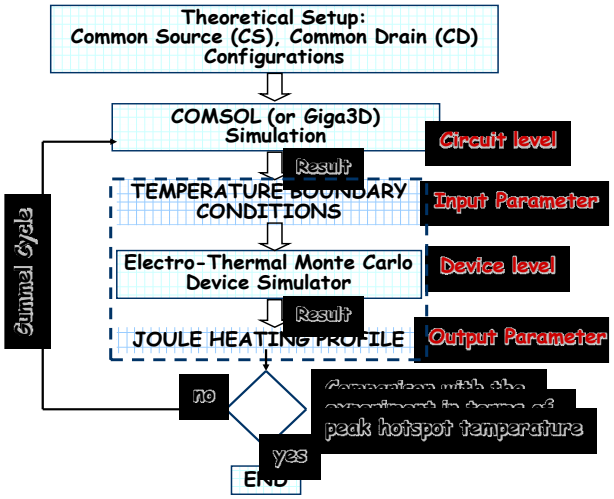

Fig. 3. Flowchart of a novel multi-scale modeling approach – an experimental-simulation procedure to properly estimate the hotspot temperature

The paper is organized as follow: in Section 2, the IMEC heater-sensor experimental procedure is explained. The electro-thermal particle based device simulator is presented in Section 3. In Section 4 simulation results for the lattice temperature profile using the proposed multiscale approach are shown. The importance of proper choice of thermal boundary conditions, in order to determine the temperature of the hot-spot, is pointed out. Conclusions and future directions of work are given in Section 5.

2. IMEC HEATER-SENSOR MEASUREMENT TECHNIQUE AND MULTISCALE MODELING APPROACH

Few measurement techniques are available for assessing self-heating induced ΔT or ΔT induced drive current reduction and many simulation efforts of this effect lack experimental support. Moreover, these classical measurement techniques convolute the self-heating effects (SHE) measurement with other device degradation mechanisms such as bias temperature instabilities (BTI), hot carrier degradation (HC) and dielectric breakdown (BD) [13–16].

IMEC proposed a unique temperature measurement technique for nanoscale MOSFET devices, based on the temperature dependence of the subthreshold slope (swing) [17]. Two different measurement configurations have been considered in this multi-scale simulation effort: common-source and common-drain configurations. Both are illustrated in Figure 4. It's a two transistor structure consisting of two *n*-channel MOSFETs: one acts as a heater (DUT = Device Under Test) and the other acting as a sensor. To uncover the hotspot temperature of the heater, the sensor shares the same active area with the heater and is separated by one poly pitch. Depending on the width of the entire structure, and the separation between the devices, the sensor will capture more or less heat of the transistor. The wide structure with the smallest gate-to-gate distance is shown to be most sensitive.

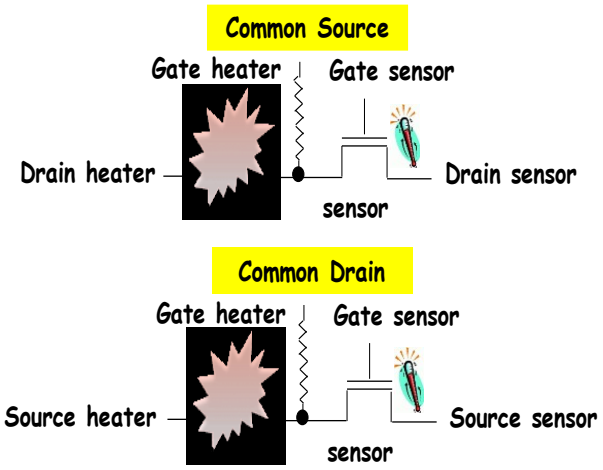

Fig. 4. The heater sensor measurement configurations of two *n*-channel MOSFETs: common source (CS) and common drain (CD). The heater (DUT = Device Under Test) operates in a saturation, while the sensor operates in a subthreshold region

The IMEC experimental procedure is as follows. To extract the temperature increase ΔT induced by the heater (or DUT), a sensor's temperature dependent characteristic is measured and subsequently, the sensor's subthreshold swing (SS) is extracted using modified EKV model [18–19]. As a calibration, the external temperature is ramped and verified that the SS shows linear dependency over a wide temperature range. Then, the heater is biased in saturation conditions (high V_D and V_G). It is found, that the subthreshold swing reduction in the sensor is proportional to the heat dissipated in the device, so the ΔT and the thermal resistance R_{TH} can be extracted. Knowing the temperature of the sensor, the next step is to perform device simulations (using COMSOL commercial simulator) that produces the

average lattice temperature profile and the Joule heating distribution in the device. The average lattice temperature in the sensor for a given input power has to match the experimentally extracted value of the temperature. Then the temperature of the hot-spot is extracted from the simulations.

In commercial device simulators, such as COMSOL, SILVACO, SYNOPSIS etc., one couples the heat conduction equation including a Joule heating source term with either the drift-diffusion or energy balance equations of the corresponding carriers that participate in transport, thus arriving at the so-called non-isothermal drift-diffusion or energy balance models [20]. The Joule heating model is a local model, and therefore can not predict properly heating effects in nanoscale devices in which non-stationary transport dominates. One can make an extension and use a hydrodynamic model for the relevant carrier type, but, the simple Joule heating source term does not account for the separate acoustic and optical phonons baths that participate in the transport of heat through the structure. To overcome this deficiency of the models implemented in commercial simulators, Lai and Majumdar [21] derived energy balance equations for the optical phonons and the acoustic phonons bath (starting from the phonon Boltzmann transport equation) that couple to the electron bath via the carrier density, carrier temperature and carrier drift velocity. Hence, a siulator is needed that overcomes these limitations and takes into consideration the optical phonon to acoustic phonon bottleneck. Such approach was implemented in our electro-thermal particle based device simulator described in more details, bellow.

3. ELECTRO-THERMAL MONTE-CARLO PARTICLE BASED DEVICE SIMULATOR

A generic flow-chart of the electro-thermal particle-based device simulator developed at Arizona State University (ASU) and Ss. Cyril and Methodius University (UKIM), is shown in Figure 5. These two groups have extended the formalism of Lai and Majumder and self-consistently coupled the 2D particle-based device simulator to the 2D energy balance equations solvers for the optical and the acoustic phonon baths (Figure 5 left panel). The exchange of variables between the two solvers is such that the drift velocity, electron density and electron temperature are input parameters to the energy balance solver. The local acoustic and optical phonon temperatures are obtained from energy balance equations solver and this information is used in conjunction with the temperature dependent scattering tables. Then, carriers are scattered according to the various scattering mechanisms incorporated in the theoretical model that corresponds to the local lattice (acoustic) and optical phonon temperatures. After the Monte Carlo device simulator reaches steady state (~5 ps), averaging of the variables is performed in the last three picoseconds.

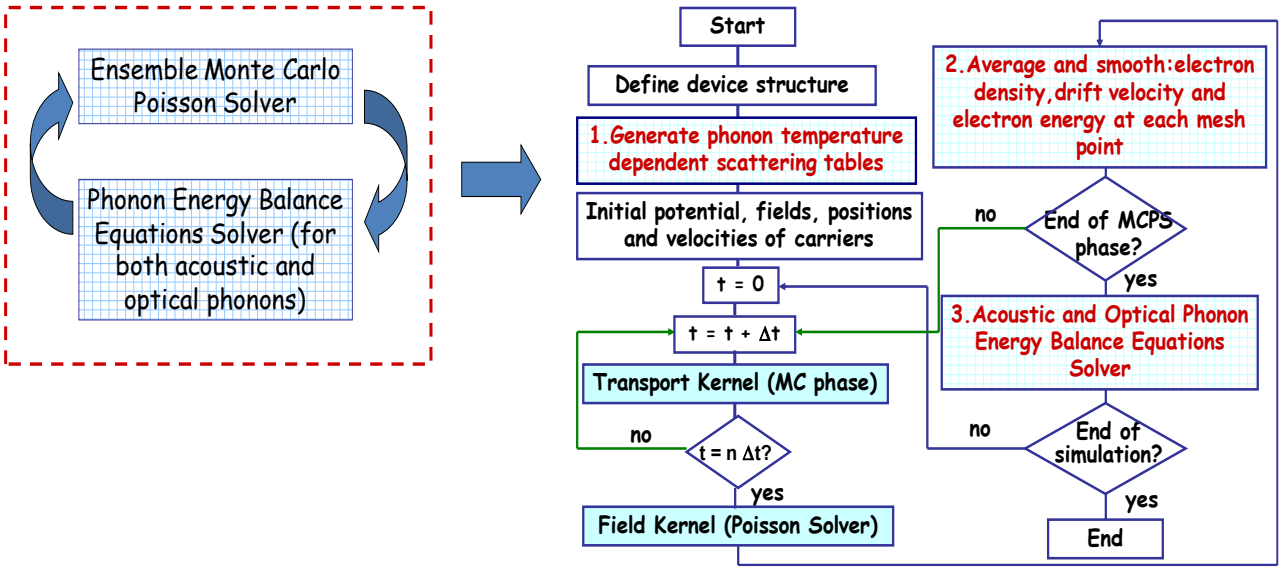

Fig. 5. Device simulator developed at ASU: the 2D Poisson equation is self-consistently solved with a Monte Carlo transport kernel and a 2D energy balance equations solvers for the acoustic (lattice) and optical phonon baths thus moving away the commonly used Joule heating model used in commercial device simulators. Such simulations give rise to more pronounced hot-spots, because they accurately represent the optical to acoustic phonon bottleneck.

Then, the drift velocity, the electron density and the electron temperature are fed back into the energy balance solver, and the whole procedure is repeated until self consistency in the current is achieved up to the third digit. It typically takes on the order of 3–5 Gummel cycles (global loops) to achieve the desired current convergence. Details of the theoretical model implemented can be found in Refs. [8, 22–23].

In our previous works, the device simulator has been used in the study of self-heating effects in nanoscale fully-depleted SOI devices. The simulation results show that in the smallest devices considered the heat is in the contacts, not in the active channel region of the device. Therefore, integrated circuits get hotter due to larger density of devices but the device performance is only slightly degraded at the smallest device size. This is because of two factors: pronounced velocity overshoot effect and smaller thermal resistance of the buried oxide layer.

In this work, according to IMEC heater-sensor configurations, the thermally coupled Monte Carlo device simulator was modified in order to co-simulate multiple devices which is a novelty for particle-based simulations (Figure 6). Both, common source and common drain configurations were studied (Figure 7), but in this section, only simulation results for common drain configuration are presented. In order to check whether the simulator is behaving according to the physical laws, we observe conservation of particles that is expressed by the fact that the source and drain currents have equal value but opposite sign. After sufficient time has elapsed, so that the system is driven into a steady-state regime, one can calculate the steady-state current through a specified terminal. The device current can be determined via two different, but consistent methods. First, by keeping track of the charges entering and exiting each terminal, the net number of charges over a period of the simulation can be used to calculate the current. The method is quite noisy due to the discrete nature of the carriers. For given bias conditions (see Figure 7) the calculated current values for two transistors are: $I_{s1} = 1.15$ mA/um, $I_{s2} = 0.039$ mA/um, $I_d = I_{s1} + I_{s2} = 1.189$ mA/um. In a second method, the sum of the carrier velocities in a portion of the device are used to calculate the current. Both methods (Figure 8) give the same value of the current through the device which suggests that conservation of particles in the system is being preserved.

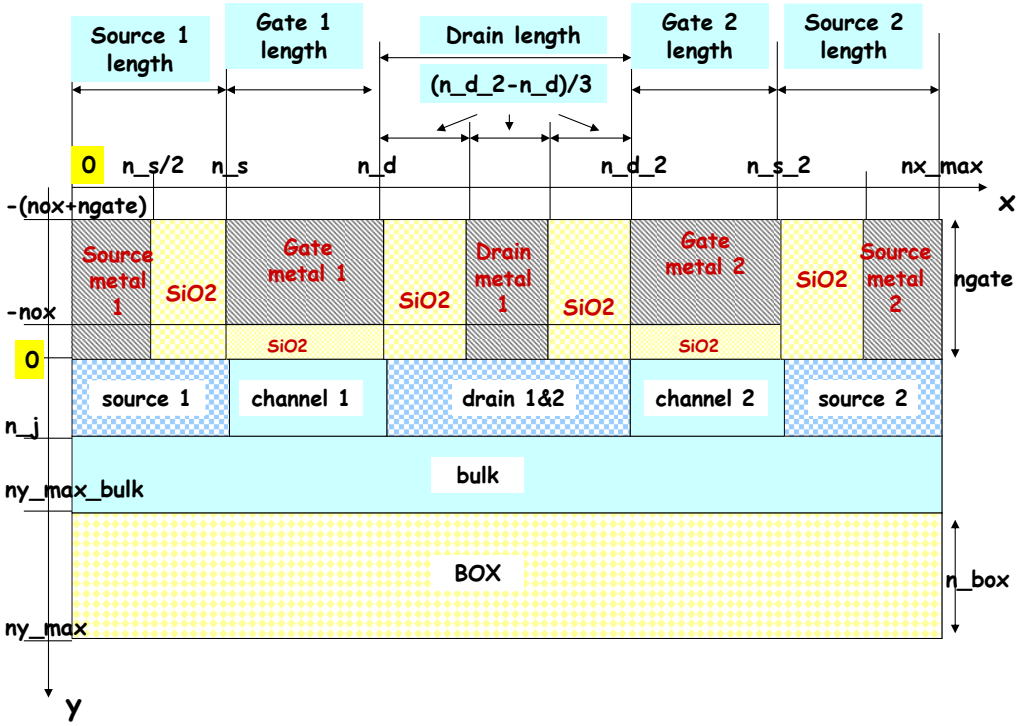

Fig. 6. Cross-section of the simulated common drain heater-sensor configuration. For the common source configuration, the drain-source regions are switched. This structure can be used for simulation of conventional and SOI (Silicon-On-Insulator) MOSFETs. In this research work, the BOX thickness (n_box) is set to zero, since the heater and the sensor are bulk MOSFET devices. The channel length for both transistors is 50 nm, with the common drain/common source length of 75 nm. The thickness of the active silicon layer is 20 nm, and the bulk thickness is 200 nm.

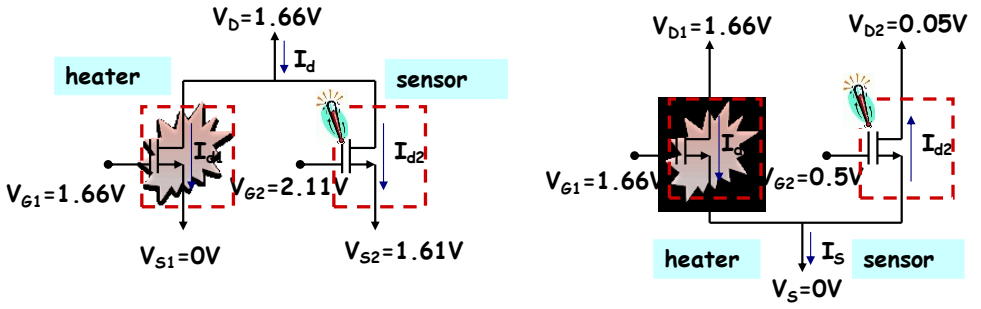

Fig. 7. Common drain (left) and common source (right) configurations with applied biases. The heater/sensor has the same bias conditions in both configurations. The power of heater in both configurations is 1mW.

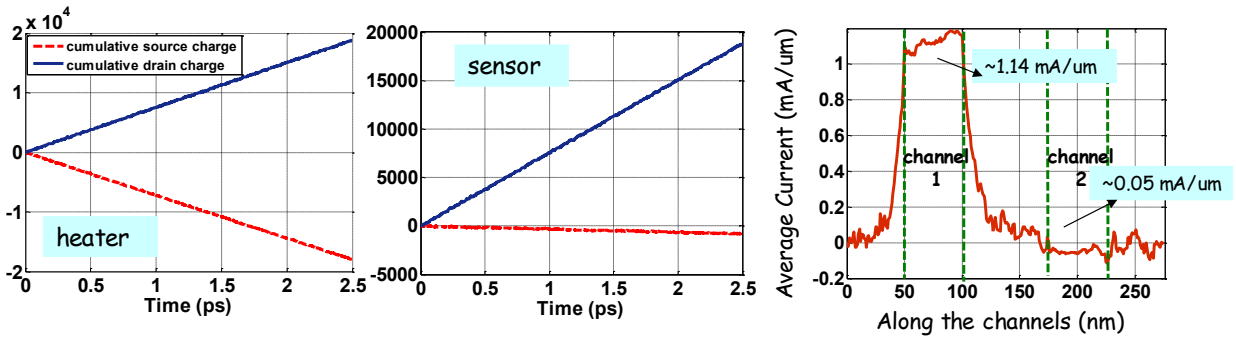

Fig. 8. Two different methods for current calculations: (1) Cumulative charge versus time for a given bias conditions in the heater (left panel) and the sensor (middle panel). The slope of the curve gives the source and drain currents. (2) Current density is calculated by using the average drift velocity of the carriers in the *x*-direction (right panel).

Simulation results shown in Figure 9 are obtained for CD configuration with bias conditions given in Figure 7. This is a visual representation of how the energy is transferred from the electron system to the lattice as depicted in Figure 2. The simulation results for the lattice (acoustic) and optical phonon temperature profiles are presented in the bottom panel of Figure 9. The hot-spot is in the channel region of the heater, near the common drain region, where are the hottest electrons. It is also evident the phonon-energy bottleneck, which can be explained by the fact that the electrons are in the velocity overshoot (vsat = 1.1×10^5 m/s) in the larger portion of the channel region in the heater (see Figure 10). The average electron energy in both devices is shown in Figure 10. To conclude from the presented results – more ballistic transport, less transfer of energy to the lattice, less heating.

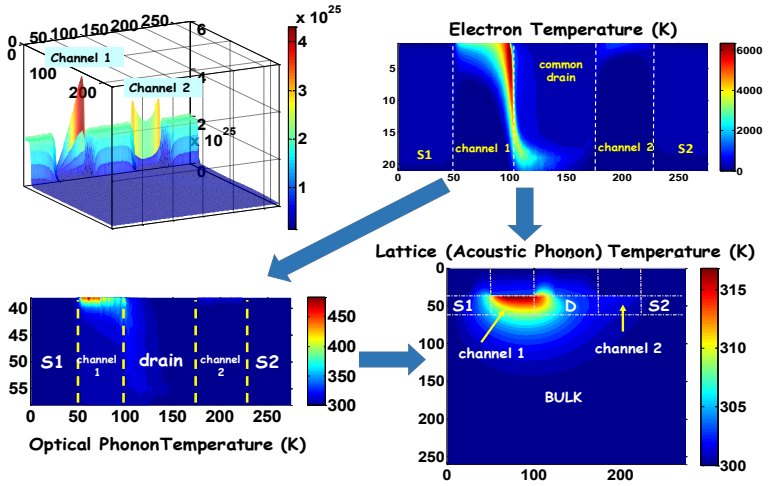

Fig. 9. CD configuration: Top panel – Electron density profile (left) and the electron temperature distribution in the active silicon layer (right). Bottom panel – Lattice temperature profile (right) and optical phonon temperature profile in the active silicon layer (left). Note the phonon-energy bottleneck

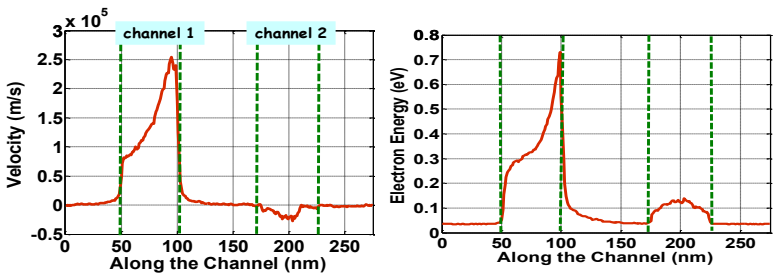

Fig. 10. Average electron velocity (left panel) and electron energy (right panel) along the channel

4. THE IMPORTANCE OF PROPER CHOICE OF THERMAL BOUNDARY CONDITIONS

To properly solve the phonon energy balance equations, the device must be attached to a heat sink somewhere along the boundary. The substrate is typically treated as a thermal contact in commercial simulation packages such as the Silvaco ATLAS (GIGA3D module) [20]. The thermal boundary conditions chosen need to reflect the physics of the individual device, as well as those in the surrounding environment. The simulation results presented in Section 3 are done assuming Dirichlet boundary conditions (constant temperature of 300 K) at the top of the metal contacts and the substrate. Different combinations of boundary conditions have been applied on the simulated structures. Simulation results show that when the top boundary (top of the metal contacts) is set to 300 K, there is almost no difference at the lattice temperature profile when Dirichlet or Neumann boundary conditions are imposed at vertical sides (no heat flux at the direction perpendicular to vertical sides). With these boundary conditions, the temperature at the sensor was much lower when compared with the results from experimental procedure.

To accurately determine the hot-spot temperature at the heater side, the thermal boundary conditions obtained from the IMEC experimental procedure were used in simulation, as shown in Figure 11.

The complete circuitry was modelled using COMSOL simulations and the boundary conditions for the active devices region was used in the thermal Monte Carlo device solver.

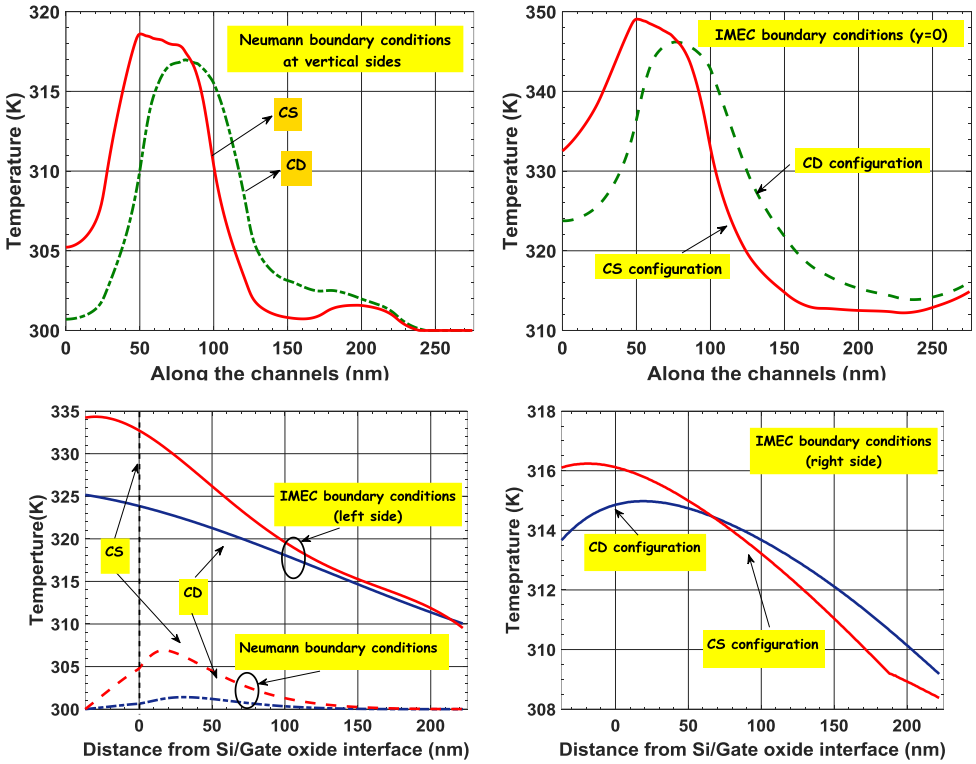

Fig. 11. Top panel: Lattice temperature profile along the channels (x-axis) at silicon/gate oxide interface for different boundary conditions. Bottom panel: Lattice temperature profile at vertical sides along y-axis. Metal contact regions are for $y < 0$. The top of the metal contact is at $y = -37$ nm.

Simulation results for the lattice temperature profile and the average lattice temperature profiles along the channel using IMEC boundary conditions are shown in Figure 12. It is clearly seen from the results presented that the magnitude of the hot-spot is larger in the common source configuration. At this point full self-consistency (the Gummel cycle) is not completely implemented. The Joule heating profile (see Figure 13) can be used as an input parameter in COMSOL simulations in order to obtain the self-consistency of the proposed multiscale approach. Nevertheless, the simulation results for the on-current and the temperature of the sensor are in very close agreement with the experimentally extracted ones.

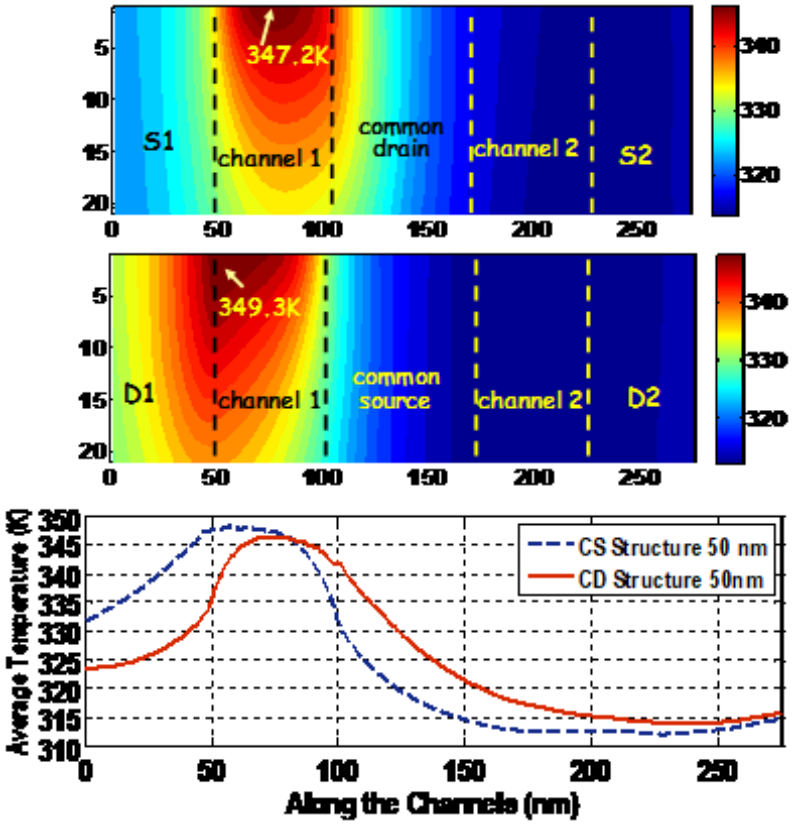

Fig. 12. Lattice temperature profile in the active silicon layer for CD (top) and CS (middle) configurations and average lattice temperature profile for both configurations (bottom) using thermal boundary conditions obtained from IMEC experimental procedure. For both configurations, the temperature at the sensor is around 315 K. Multi-scale approach has been used in obtaining these results.

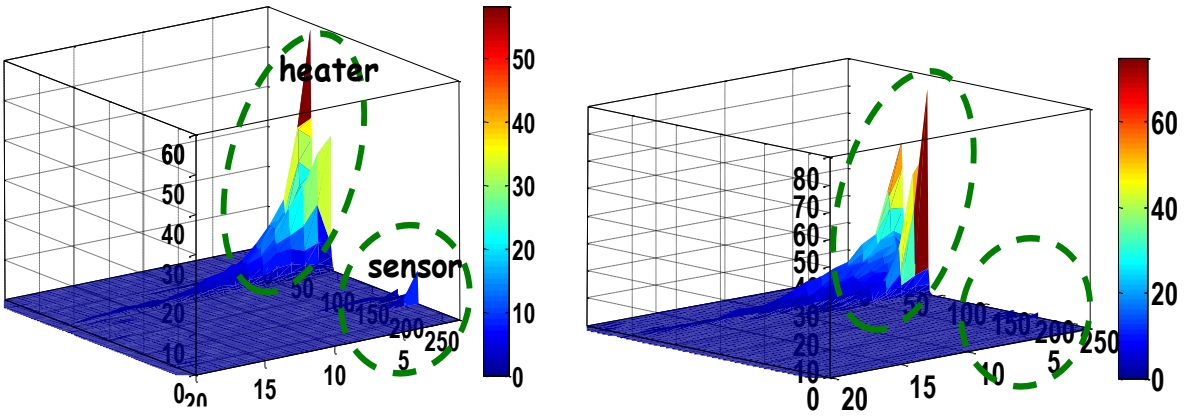

Fig. 13. Joule heat profile (W/um^3) for CD (left) and CS (right) configurations. This profile is an input parameter for COMSOL device simulator

It is obvious that, using the top boundary as a heat sink (set to 300 K) is not a proper choice for boundary conditions, because it underestimates the hot-spot temperature and the sensor cannot detect any increase of the temperature (see Figure 11). Using Neumann boundary conditions at the top boundary, except at the source metal contact of the sensor, gives more realistic results for the hot-spot temperature as shown in Figure 14. However, if we compare the results of the temperature profiles along the silicon/gate oxide interface and the top of the metal contacts for Neumann boundary conditions with the results of IMEC boundary conditions (Figure 15), one can conclude that, even when the heat flux is not allowed at the direction perpendicular to the top boundary, the temperature of the top boundary is lower than the temperature obtained from IMEC experimental procedure which leads to lower heater temperature and the sensor that has a temperature of 301 K. Therefore, the role of interconnect self-heating has to be accounted for.

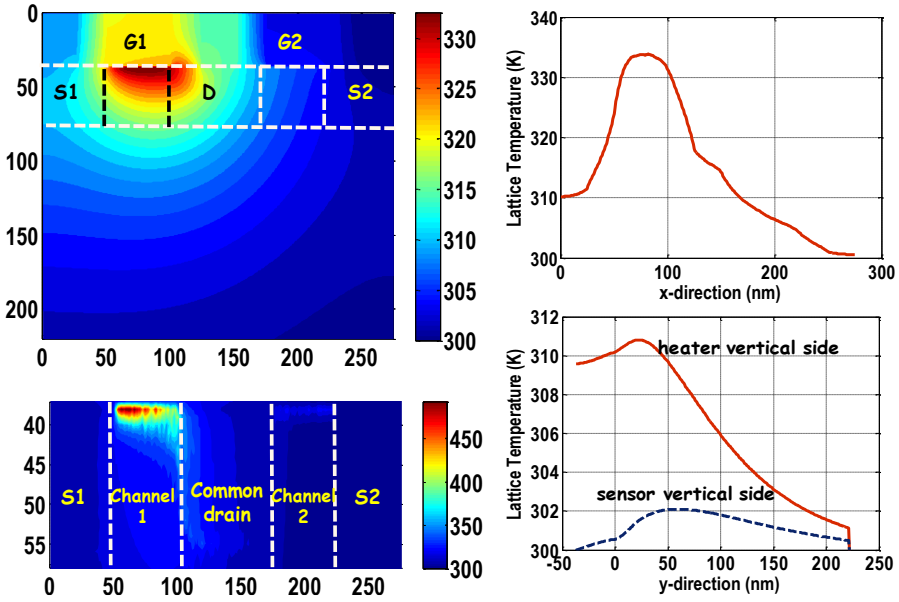

Fig. 14. CD configuration simulation results using Neumann boundary conditions, except at the source side of the sensor and the bottom boundary where temperature is set to 300 K. The calculated currents for the heater and the sensor matched the values obtained with IMEC boundary conditions: $I_{s1} = 1.351$ mA/um, $I_{s2} = 0.136$ mA/um, $I_d = I_{s1} + I_{s2} = 1.487$ mA/um.

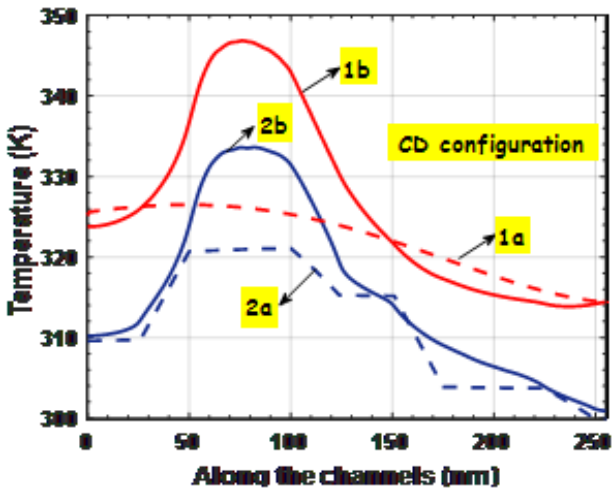

Fig. 15. CD configuration: 1a – Lattice temperature profile at the top of the metal contacts (IMEC boundary conditions); 1b – Lattice temperature profile along the Si/gate oxide interface (IMEC boundary conditions); 2a – Lattice temperature profile at the top of the metal contacts (Neumann boundary conditions at the top of the metal contacts, except $T = 300$ K at source metal contact of the sensor); 2b – Lattice temperature profile along the Si/gate oxide interface for boundary conditions of 2a

5. CONCLUSIONS

In this work we demonstrate: 1) that we can co-simulate multiple devices with our thermally coupled Monte Carlo device simulator; and 2) that the synergy of experiment and theory can give quite accurate values for the temperature of the hot-spot in conventional planar MOSFETs.

Efficient removal of heat from the metal contacts is still an unsolved problem and can lead to a variety of non-desirable effects, including electromigration. Therefore, it is important to account for heating effects not only in the device itself, but also in the contacts and interconnects when considering system reliability. For this purpose, another level of hierarchy in the multi-scale modeling approach is introduced. Giga 3D (Silvaco Atlas module) is used to model the role of interconnects and the role of the larger simulation domain and is also used to extract the temperature boundary conditions for a smaller domain electro-thermal device simulator. The electro-thermal simulator passes Joule heating terms to Giga 3D and the whole Gummel iteration loop is repeated until a self-consistent solution at multiple levels of approximation is achieved. The results of this research work will be presented elsewhere.

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